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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,131	10/30/2003	Steve James Ungstad	10030410-1	9970

7590 04/15/2004

AGILENT TECHNOLOGIES, INC.
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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,131	UNGSTAD, STEVE JAMES	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-14* is/are allowed.

6)☒ Claim(s) *1,3,5 and 8* is/are rejected.

7)☒ Claim(s) *2,4 and 9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-14 are presented in the instant application according to the Applicant' filing on 10/30/2003.

Claim Objections/Minor Informalities

1. Claim 1 is objected to because of the following informalities:

Line 4, there is no express antecedent basis for "the reference clock signal". It is suggested that "the" be changed to -- a -- .

Line 6, antecedent for " a reference clock signal" has already been recited in line 4 (from previous correction). It is suggested that "a" be changed to –the --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 3, 5, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Dalmia (U.S. Patent No. 6,683, 930).

With respect to claims 1 and 3, Dalmia discloses, in Figure 4, a method of distributing a clock signal, the method comprising the steps of a) generating an output clock signal [RECVD_CLK] onto a transmission line *(this is inherent since the generated output clock is to be distributed to other elements for example in a synchronous memory device, see Kyung et al. U.S. Patent No. 6,072,846 (col. 1, lines 27-32))* and obtaining a returned clock signal from a return line matched to the transmission line; b) detecting [104] a returned clock signal [118]; c) detecting [102] a first phase difference between the reference clock signal [DATA] and the output clock signal [RECVD_CLK]; d) detecting [104] a second phase difference between a reference clock signal [DATA] and the returned clock signal [118]; e) controlling [110] the phase of the output clock signal based on an average of the first and second phase differences.

With respect to claim 5, Dalmia discloses, in Figure 4, that the step of controlling the phase of the output clock signal comprises driving a voltage controlled oscillator [110] using the average of the first and second phase differences.

With respect to claim 8, Dalmia discloses, in Figure 4, a clock distribution circuit comprising a) a first phase detector [102] that outputs a phase lead of an output clock signal; b) a second phase detector [104] that outputs a phase lag of a returned clock signal; and c) circuitry [110] that propagates the output clock signal onto a transmission line *(this is inherent since the generated output clock is to be distributed to other elements for example in a synchronous memory device, see Kyung et al. U.S. Patent No. 6,072,846 (col. 1, lines 27-32))* based on the average the output of the first phase detector and the second phase detector.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dalmia (U.S. Patent No. 6,683,930) in view of Hill et al. (U.S. Patent No. 6,002,284).

With respect to claim 6, Dalmia discloses all of the claimed limitations as expressly recited in claim 1, except for the method further comprising the step of buffering the output of the voltage controlled oscillator.

Koike discloses, in Fig. 1, a phase locked loop system [60] including a buffer [64] being coupled to a voltage controlled oscillator [63].

To modify the circuit of Dalmia by additionally coupling a buffer to a voltage controlled oscillator for providing a balanced voltage controlled oscillator output, as taught by Koike, would have been obvious to one of ordinary skill in the art at the time of the invention since Koike teaches that such a configuration would prevent the effect of the resonance frequency of the next stage on from being fed back to the voltage controlled oscillator *(see Koike, col. 6, lines 27-31).*

Allowable Subject Matter

6. Claims 12-14 are allowed.

7. Claims 2, 4, 7 and 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest:

- A method of distributing clock including the step of obtaining the returned clock signal by sensing a reflection of the output clock signal on the transmission line, as called for in claim 2;

- A method of distributing clock further including the step of comprising buffering the output of the voltage controlled oscillator and providing a build out impedance to match the transmission-line impedance, as called for in claim 7;

- The clock distribution circuit further including circuitry to detect the returned clock signal as a reflected clock signal on the transmission line, as called for in claim 9;

- The clock distribution circuit further including a signal return line separate from the transmission line, in which the returned clock signal is sensed from the signal return line, as called for in claim 10;

- A clock distribution circuit including second circuitry that propagates the first output clock signal onto a second transmission line based on the average the output of the third phase detector and the fourth phase detector, in combination with the remaining claimed limitations, as called for in independent claim 12;

• A method of distributing a reference clock signal, the method including the steps of a) Sensing a reflected clock signal at the beginning of the transmission line, and b) adjusting the output clock signal based on an average of a first phase difference between the output clock signal and the reference clock signal and a second phase difference between the reflected clock signal and the reference clock signal, as called for in independent claim 13; and

• A method of distributing a reference clock signal, the method including the steps of a) sensing a returned clock signal at the end of a signal return line matched to the transmission line, and b) adjusting the output clock signal based on an average of a first phase difference between the output clock signal and the reference clock signal and a second phase difference between the returned clock signal and the reference clock signal, as called for in independent claim 14.

Citation of Relevant Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Lee et al. (U.S. Patent No. 6,704,383) discloses a sample and hold type fractional-N frequency synthesizer.

Prior art Everitt et al. (U.S. Patent No. 6,577,695) discloses an emulating narrow band phase-locked loop behavior on a wide band phase-locked loop.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen
Examiner
Art Unit 2816

LMN